TOSHIBA CMOS Digital Integrated Circuit　Silicon Monolithic

TC74LVX32F,TC74LVX32FN,TC74LVX32FT

Quad 2-Input OR Gate

The TC74LVX32F/ FN/ FT is a high-speed CMOS 2-input OR gate fabricated with silicon gate CMOS technology. Designed for use in 3-V systems, it achieves high-speed operation while maintaining the CMOS low power dissipation.

This device is suitable for low-voltage and battery operated systems.

The internal circuit is composed of 4 stages including buffer output, which provide high noise immunity and stable output.

An input protection circuit ensures that 0 to 5.5V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5V to 3V systems and two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.
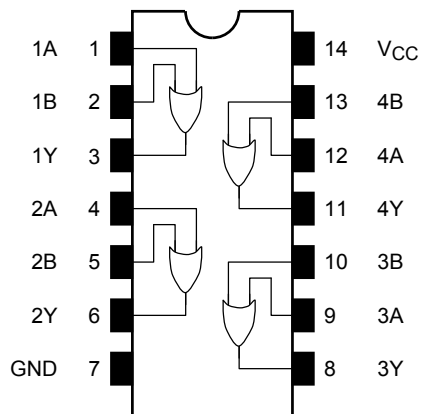
Features

- High-speed: $t_{pd} = 4.4$ ns (typ.) ($V_{CC} = 3.3$ V)
- Low power dissipation: $I_{CC} = 2$ μA (max) (Ta = 25°C)
- Input voltage level: $V_{IL} = 0.8$ V (max) ($V_{CC} = 3$ V)

  $V_{IH} = 2.0$ V (min) ($V_{CC} = 3$ V)
- Power-down protection provided on all inputs
- Balanced propagation delays: $t_{pLH} \simeq t_{pHL}$
- Low noise: $V_{OLP} = 0.5$ V (max)
- Pin and function compatible with 74HC32

Note:　xxxFN (JEDEC SOP) is not available in Japan.

TC74LVX32F

SOP14-P-300-1.27A

SOP14-P-300-1.27

TC74LVX32FN

SOL14-P-150-1.27

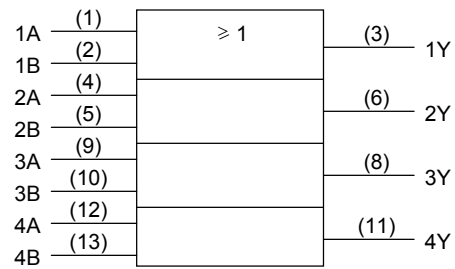TC74LVX32FT
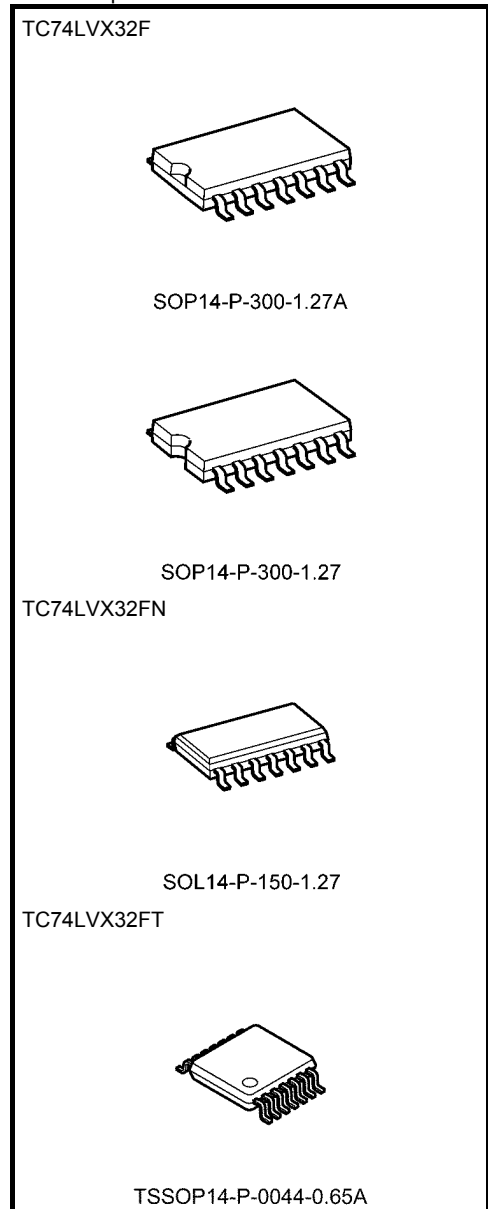
TSSOP14-P-0044-0.65A

Weight

SOP14-P-300-1.27A	: 0.18 g (typ.)
SOP14-P-300-1.27	: 0.18 g (typ.)
SOL14-P-150-1.27	: 0.12 g (typ.)
TSSOP14-P-0044-0.65A	: 0.06 g (typ.)

Pin Assignment (top view)

1A	1		14	V_CC
1B	2		13	4B
1Y	3		12	4A
2A	4		11	4Y
2B	5		10	3B
2Y	6		9	3A
GND	7		8	3Y

IEC Logic Symbol

		≥ 1		
1A	(1)		(3)	1Y
1B	(2)			
2A	(4)		(6)	2Y
2B	(5)			
3A	(9)		(8)	3Y
3B	(10)			
4A	(12)		(11)	4Y
4B	(13)			

Truth Table

Inputs		Outputs
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	H

Absolute Maximum Ratings (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage range	V_{CC}	−0.5 to 7.0	V
DC input voltage	V_{IN}	−0.5 to 7.0	V
DC output voltage	V_{OUT}	−0.5 to V_{CC} + 0.5	V
Input diode current	I_{IK}	−20	mA
Output diode current	I_{OK}	±20	mA
DC output current	I_{OUT}	±25	mA
DC V_{CC}/ground current	I_{CC}	±50	mA
Power dissipation	P_D	180	mW
Storage temperature	T_{stg}	−65 to 150	°C

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Recommended Operating Conditions (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage	V_{CC}	2.0 to 3.6	V
Input voltage	V_{IN}	0 to 5.5	V
Output voltage	V_{OUT}	0 to V_{CC}	V
Operating temperature	T_{opr}	−40 to 85	°C
Input rise and fall time	dt/dv	0 to 100	ns/V

Note: The recommended operating conditions are required to ensure the normal operation of the device.
Unused inputs must be tied to either VCC or GND.

Electrical Characteristics

DC Characteristics

Characteristics		Symbol	Test Condition		V_{CC} (V)	Ta = 25°C			Ta = −40 to 85°C		Unit
						Min	Typ.	Max	Min	Max	
Input voltage	H-level	V_{IH}	—		2.0	1.5	—	—	1.5	—	V
					3.0	2.0	—	—	2.0	—	
					3.6	2.4	—	—	2.4	—	
	L-level	V_{IL}	—		2.0	—	—	0.5	—	0.5	
					3.0	—	—	0.8	—	0.8	
					3.6	—	—	0.8	—	0.8	
Output voltage	H-level	V_{OH}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -50\ \mu A$	2.0	1.9	2.0	—	1.9	—	V
				$I_{OH} = -50\ \mu A$	3.0	2.9	3.0	—	2.9	—	
				$I_{OH} = -4\ mA$	3.0	2.58	—	—	2.48	—	
	L-level	V_{OL}	$V_{IN} = V_{IL}$	$I_{OL} = 50\ \mu A$	2.0	—	0	0.1	—	0.1	
				$I_{OL} = 50\ \mu A$	3.0	—	0	0.1	—	0.1	
				$I_{OL} = 4\ mA$	3.0	—	—	0.36	—	0.44	
Input leakage current		I_{IN}	$V_{IN} = 5.5$ V or GND		3.6	—	—	±0.1	—	±1.0	μA
Quiescent supply current		I_{CC}	$V_{IN} = V_{CC}$ or GND		3.6	—	—	2.0	—	20.0	μA

AC Characteristics (input: $t_r = t_f = 3$ ns)

Characteristics	Symbol	Test Condition			Ta = 25°C			Ta = −40 to 85°C		Unit
			V_{CC} (V)	C_L (pF)	Min	Typ.	Max	Min	Max	
Propagation delay time	t_{pLH}	—	2.7	15	—	5.8	10.7	1.0	13.5	ns
				50	—	8.3	14.2	1.0	17.0	
	t_{pHL}		3.3 ± 0.3	15	—	4.4	6.6	1.0	8.0	
				50	—	6.9	10.1	1.0	11.5	
Output to output skew	t_{osLH}	(Note 1)	2.7	50	—	—	1.5	—	1.5	ns
	t_{osHL}		3.3 ± 0.3	50	—	—	1.5	—	1.5	
Input capacitance	C_{IN}	(Note 2)			—	4	10	—	10	pF
Power dissipation capacitance	C_{PD}	(Note 3)			—	14	—	—	—	pF

Note 1: Parameter guaranteed by design.
  ($t_{osLH} = |t_{pLHm} − t_{pLHn}|$, $t_{osHL} = |t_{pHLm} − t_{pHLn}|$)

Note 2: Parameter guaranteed by design.

Note 3: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption.
  Average operating current can be obtained by the equation:
  $I_{CC\,(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4$ (per gate)

Noise Characteristics (Ta = 25°C, input: $t_r = t_f = 3$ ns, $C_L = 50$ pF)

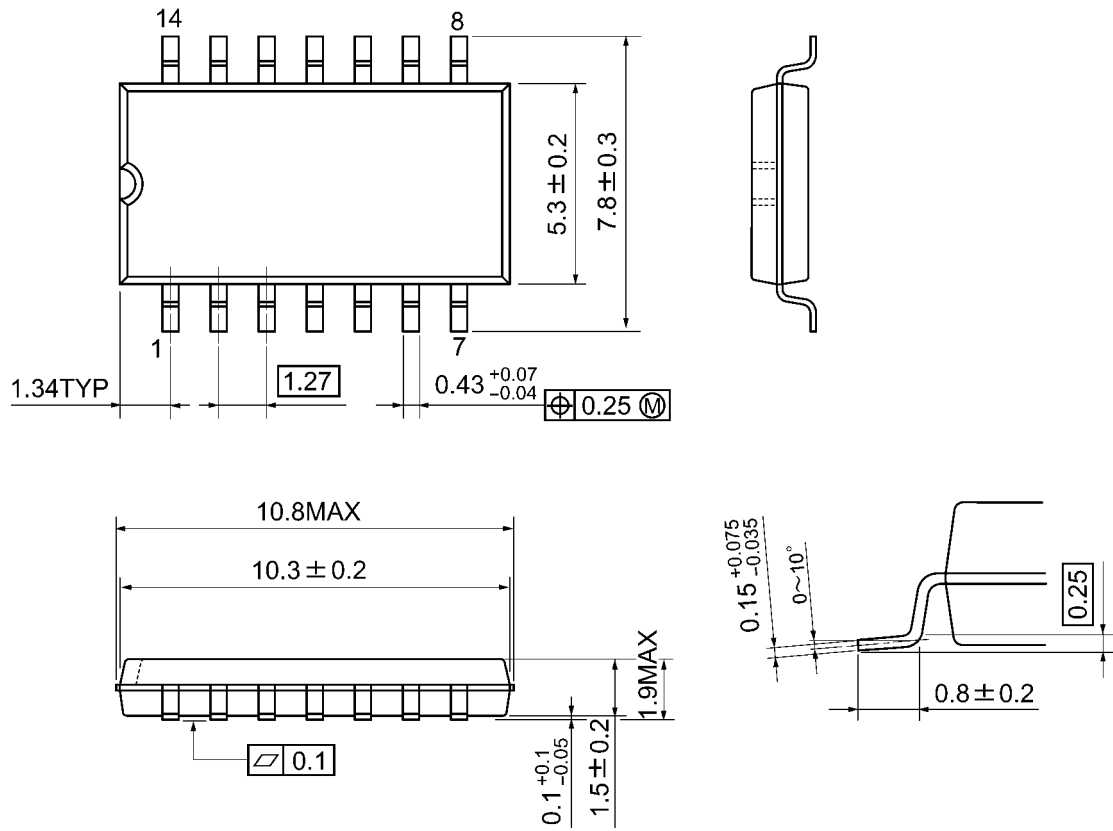| Characteristics	Symbol	Test Condition	V_{CC} (V)	Typ.	Limit	Unit
Quiet output maximum dynamic V_{OL}	V_{OLP}	—	3.3	0.3	0.5	V
Quiet output minimum dynamic V_{OL}	V_{OLV}	—	3.3	−0.3	−0.5	V
Minimum high level dynamic input voltage V_{IH}	V_{IHD}	—	3.3	—	2.0	V
Maximum low level dynamic input voltage V_{IL}	V_{ILD}	—	3.3	—	0.8	V

Input Equivalent Circuit
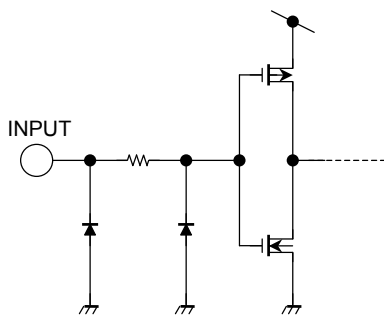
Package Dimensions

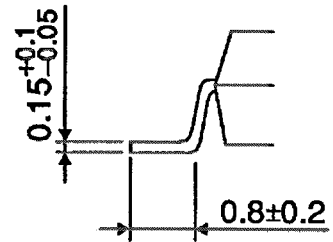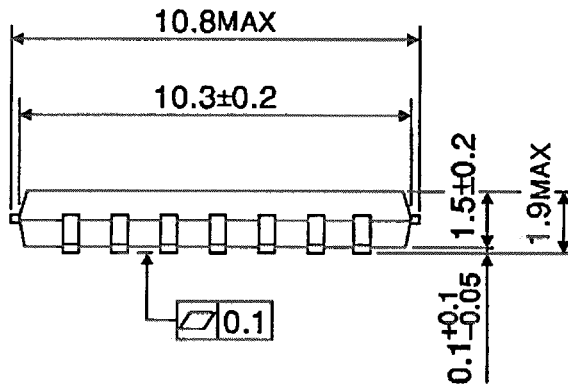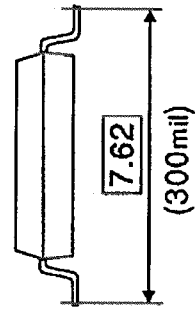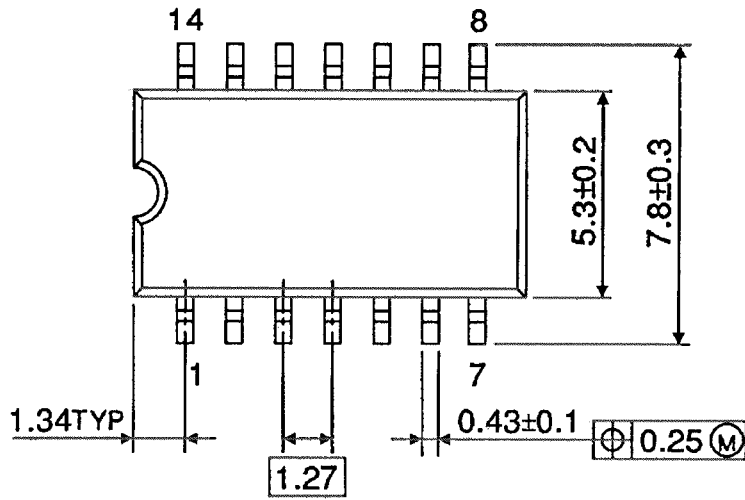SOP14-P-300-1.27A   Unit: mm

Weight: 0.18 g (typ.)

Package Dimensions

SOP14-P-300-1.27

Unit : mm

14 8

5.3±0.2

7.8±0.3

1

7

1.34TYP

0.43±0.1

⊕ 0.25 Ⓜ

1.27

7.62

(300mil)

10.8MAX

10.3±0.2

1.5±0.2

1.9MAX

$0.1^{+0.1}_{-0.05}$

⟋ 0.1

$0.15^{+0.1}_{-0.05}$

0.8±0.2

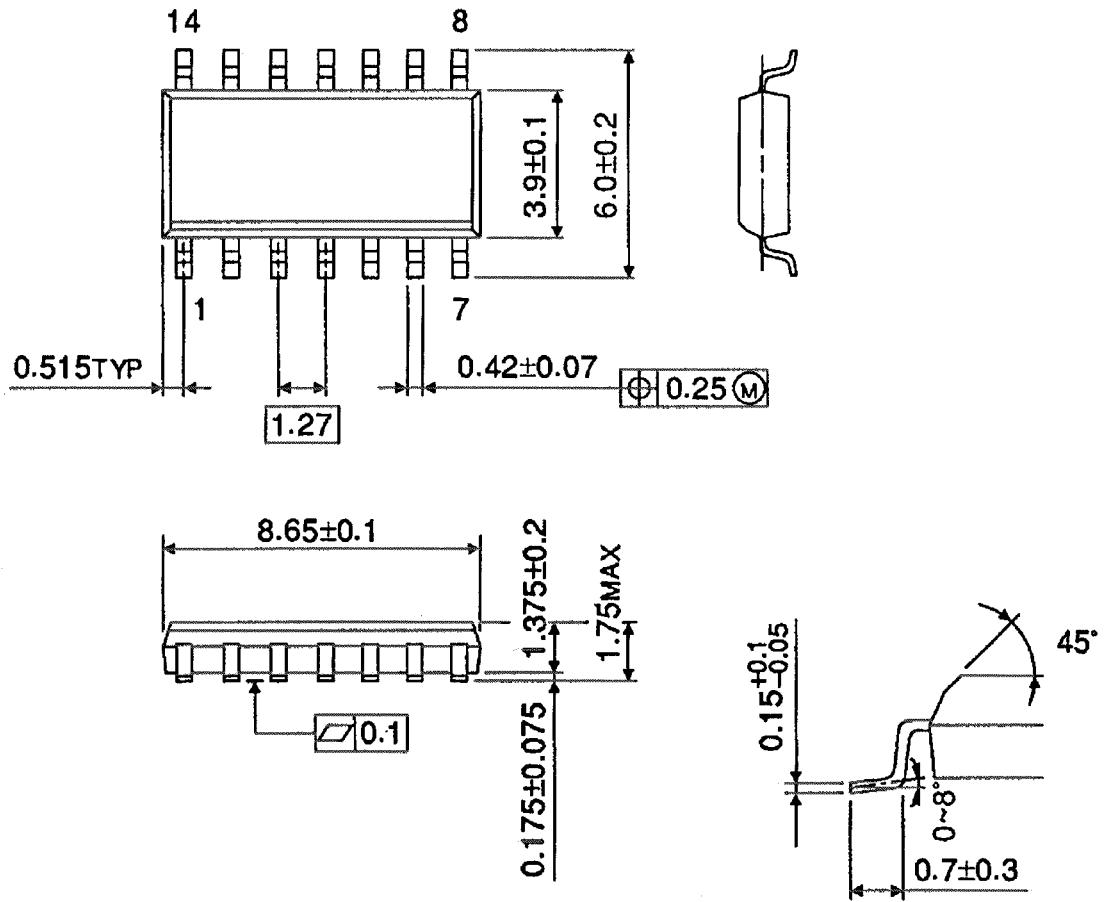Weight: 0.18 g (typ.)

Package Dimensions (Note)

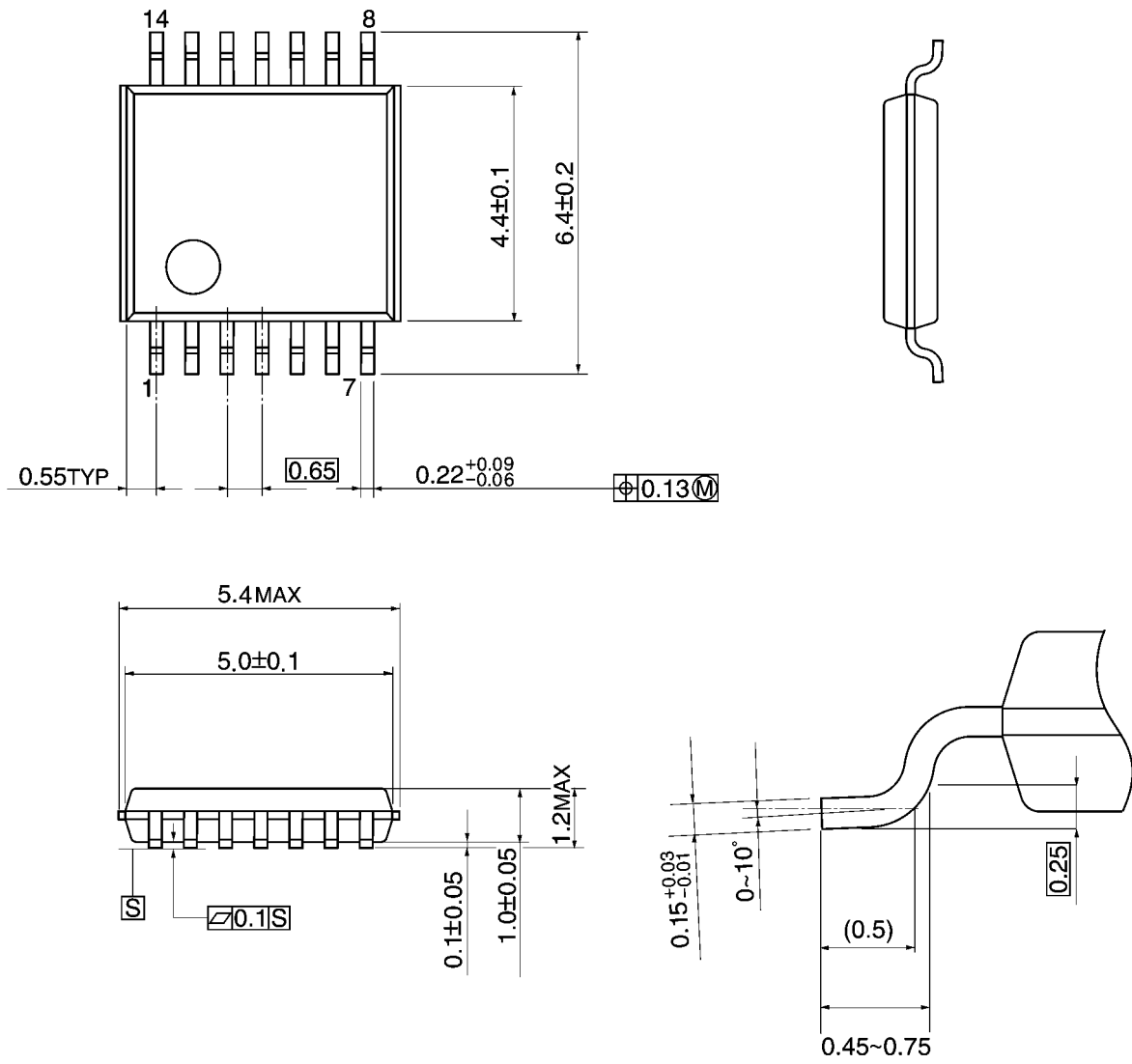SOL14-P-150-1.27   Unit : mm

Note: This package is not available in Japan.

Weight: 0.12 g (typ.)

Package Dimensions

TSSOP14-P-0044-0.65A

Unit: mm

14   8

4.4±0.1

6.4±0.2

1   7

0.55TYP   0.65   0.22$^{+0.09}_{-0.06}$ ⌖ 0.13Ⓜ

5.4MAX

5.0±0.1

1.2MAX

S   ⟋0.1S

0.1±0.05   1.0±0.05

0.15$^{+0.03}_{-0.01}$ 0~10°   0.25

(0.5)

0.45~0.75

Weight: 0.06 g (typ.)

Note: Lead (Pb)-Free Packages

SOP14-P-300-1.27A   SOL14-P-150-1.27   TSSOP14-P-0044-0.65A

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20070701-EN

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